Hiral Matehuala

ASIC Design Engineer

Dedicated ASIC Design Engineer with 1 year of experience in designing and verifying digital systems for integrated circuits. Proficient in RTL design, SystemVerilog, and FPGA programming, with a strong foundation in digital logic and hardware description languages. Adept at optimizing designs for performance, power, and area, while effectively collaborating within cross-functional teams. Eager to contribute to innovative projects and continuously expand technical skillset in the field of ASIC design.

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123 Oak Street, Charlotte, NC 28205

Education

Master of Science in Electrical and Computer Engineering at North Carolina State University, Raleigh, NC

Aug 2018 - May 2022

Relevant Coursework: Advanced Digital Systems, VLSI Design, Embedded Systems, Computer Architecture, Analog and Digital Communication, Control Systems, Power Electronics, Microelectronics, Antennas and Propagation, Signal Processing, and Machine Learning for Engineers.

Links

linkedin.com/in/hiralmatehuala

Skills

- VHDL
- Verilog
- SystemVerilog
- Cadence Virtuoso
- Synopsys Design Compiler
- SPICE simulation

Employment History

ASIC Design Engineer at Analog Devices, NC

Mar 2023 - Present

- Successfully designed and implemented a high-performance, low-power ADC for a flagship product, resulting in a 20% reduction in power consumption and a 15% increase in overall performance.
- Led a team of 5 engineers to develop a custom ASIC for a critical automotive safety application, delivering the project on time and within budget while meeting stringent industry standards for reliability and performance.
- Innovated and patented a novel circuit design technique that increased the efficiency of voltage regulators by 25%, enabling the company to secure a major contract with a leading consumer electronics manufacturer.

Junior ASIC Design Engineer at Xilinx, NC

Aug 2022 - Jan 2023

- Successfully designed and implemented a high-performance ASIC for a complex FPGA system, resulting in a 20% increase in overall system performance and a 15% reduction in power consumption.
- Optimized the verification process for a critical ASIC design project, leading to a 30% reduction in verification time and a 10% improvement in design quality, significantly contributing to meeting project deadlines.
- Collaborated with the team to develop an innovative, low-power ASIC design methodology, which was adopted across multiple projects and resulted in a 25% reduction in power consumption for targeted designs.

Certificates

Certified Verification Engineer (CVE)

Jun 2021

Advanced VLSI Design and Test Certification

Apr 2020

Memberships

Institute of Electrical and Electronics Engineers (IEEE)