ELLISA PEREZFLORES

ASIC Engineer

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(245) 773-4668
123 Main St, Wichita, KS 67202

PROFILE

Dedicated ASIC Engineer with 1 year of experience in designing and verifying complex digital systems. Proficient in RTL design, simulation, and synthesis, with a strong foundation in programming languages such as Verilog, VHDL, and SystemVerilog. Adept at collaborating cross-functionally to achieve project goals and continuously improve processes. Demonstrated ability to quickly learn and adapt to new technologies, delivering high-quality results in fast-paced environments.

LINKS

linkedin.com/in/ellisaperezflores

SKILLS

- VHDL
- Verilog
- SystemVerilog
- Cadence Virtuoso
- Synopsys Design Compiler
- SPICE simulation
- Static Timing Analysis

LANGUAGES

- English
- Urdu

HOBBIES

EMPLOYMENT HISTORY

ASIC Design Engineer at Garmin International Inc., KS

Apr 2023 - Present

- Led a team of 5 engineers in the successful design and implementation of a high-performance ASIC chip for Garmin's latest GPS device, resulting in a 20% increase in processing speed and a 15% reduction in power consumption.
- Developed an innovative power management system for ASIC devices, which reduced power consumption by 25% and extended battery life in Garmin's wearable products by 30%.
- Played a crucial role in the design and development of a custom ASIC solution for Garmin's aviation division, enabling a 50% reduction in size and weight of avionics systems while maintaining high levels of reliability and performance.
- Implemented advanced verification techniques for ASIC designs, leading to a 40% reduction in verification time and a 30% decrease in design iterations, significantly improving time-to-market for Garmin's products.

Junior ASIC Design Engineer at NetApp, KS

Sep 2022 - Mar 2023

- Successfully designed and implemented a high-performance ASIC module for NetApp's flagship storage system, resulting in a 20% increase in overall system performance and contributing to a 15% growth in sales revenue.
- Led a team of 5 engineers to optimize ASIC design flow, reducing the average time-to-market by 25% and enabling NetApp to stay ahead of its competitors in the rapidly evolving data storage market.
- Developed a comprehensive verification environment for ASIC designs, increasing test coverage by 30% and reducing the number of post-silicon bugs by 40%, significantly improving product quality and customer satisfaction.

EDUCATION

Master of Science in Electrical and Computer Engineering at Kansas State University, Manhattan, KS

Aug 2018 - May 2022

Relevant Coursework: Advanced Digital Systems, VLSI Design, Computer Networks, Embedded Systems, Electronic Circuits, Power Electronics, Control Systems, Digital Signal Processing, Microelectronics, and Communication Systems.

CERTIFICATES

Certified Verification Engineer (CVE)

Sep 2021