Sherise Lourido

ASIC Verification Engineer

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(334) 305-6028
123 Maple Street, Concord, NH 03301

Education

Master of Science in Electrical and Computer Engineering at University of New Hampshire, Durham, NH

Sep 2018 - May 2022

Relevant Coursework: Advanced Digital Signal Processing, VLSI Design, Computer Architecture, Wireless Communications, Embedded Systems, Machine Learning for Engineers, Power Electronics, Electromagnetic Theory, Control Systems, and Optical Networks.

Links

linkedin.com/in/sheriselourido

Skills

- SystemVerilog
- UVM (Universal Verification Methodology)
- Formal Verification
- Assertion-Based Verification (ABV)
- VHDL (VHSIC Hardware Description Language)
- FPGA Prototyping
- Coverage-Driven Verification

Languages

English

Profile

Results-driven ASIC Verification Engineer with 1 year of experience in the design and verification of digital systems. Proficient in RTL coding, test bench development, and simulation tools. Adept at collaborating with cross-functional teams to ensure high-quality, on-time project deliverables. Passionate about developing innovative solutions to improve design processes and optimize performance.

Employment History

ASIC Verification Engineer at Ansys Inc., NH

Feb 2023 - Present

- Led a team in the successful verification of a complex ASIC design, resulting in a 20% reduction in design errors and a 15% improvement in time-to-market for the product.
- Developed and implemented a new verification methodology that increased test coverage by 25%, leading to a significant improvement in overall product quality and reliability.
- Streamlined the verification process by automating key tasks, which led to a 30% reduction in man-hours and a 10% increase in overall team productivity.

Junior ASIC Verification Engineer at BAE Systems, NH

Sep 2022 - Jan 2023

- Successfully executed over 15 complex ASIC verification projects, leading to a 30% increase in overall efficiency and performance of the team.
- Developed and implemented a comprehensive test plan and testbench for a state-of-the-art ASIC design, resulting in a 20% reduction in verification time and a 10% improvement in the final product quality.
- Collaborated with cross-functional teams on a high-profile project, contributing to a 25% increase in project completion speed and earning recognition for outstanding teamwork and technical expertise.

Certificates

Advanced Verification with SystemVerilog OOP Testbench (SVTB)

Jan 2022

Universal Verification Methodology (UVM) Certificate

May 2020

Memberships

Institute of Electrical and Electronics Engineers (IEEE)

Design Automation Conference (DAC)