SATINA KIRIHARA

Fpga Design Engineer

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PROFILE

FPGA Design Engineer with 1 year of experience in designing, implementing, and verifying digital systems using FPGA platforms. Proficient in VHDL and Verilog coding, skilled in using Xilinx and Altera design tools, and adept at RTL design, simulation, and synthesis. Demonstrated ability to analyze system requirements, develop engineering specifications, and collaborate effectively with cross-functional teams. Committed to delivering innovative, high-quality solutions to meet project objectives within tight deadlines.

LINKS

linkedin.com/in/satinakirihara

SKILLS

- VHDL
- Verilog
- SystemVerilog
- High-Level Synthesis (HLS)
- ModelSim
- Xilinx Vivado
- Quartus Prime

LANGUAGES

- English
- Japanese

HOBBIES

EMPLOYMENT HISTORY

FPGA Design Engineer at Xilinx, Inc., IL

May 2023 - Present

- Developed and implemented a high-performance FPGA design for a major client, resulting in a 30% increase in processing speed and a 25% reduction in power consumption.
- Successfully led a team of 5 engineers in the completion of a complex FPGA project within a tight 6-month deadline, delivering the final product on time and within budget.
- Designed and optimized a custom IP core for a high-speed communication protocol, improving data transfer rates by 40% and enabling seamless integration into existing systems.
- Introduced innovative design techniques and tools that increased overall team productivity by 20%, leading to faster project completion times and higher quality deliverables.

Associate FPGA Design Engineer at Intel Corporation, IL

Jul 2022 - Apr 2023

- Developed and optimized a high-performance FPGA design for a critical Intel project, resulting in a 25% reduction in power consumption and a 15% improvement in performance compared to the previous solution.
- Successfully completed a complex FPGA integration for a cutting-edge AI accelerator product, which contributed to a 30% increase in overall system performance and enabled Intel to secure a $10 million contract with a major client.
- Led a team of 4 engineers in the design, implementation, and verification of a custom digital signal processing (DSP) module for an FPGA-based communication system, ultimately reducing development time by 20% and improving signal quality by 10%.
- Developed and implemented a new FPGA design methodology that incorporated automated testing and continuous integration techniques, resulting in a 50% reduction in design iteration time and a 40% decrease in bug-related issues for the entire team.

EDUCATION

Bachelor of Science in Electrical and Computer Engineering with a focus on FPGA Design at University of Illinois at Urbana-Champaign, IL

Aug 2018 - May 2022

Relevant Coursework: Digital Logic Design, VHDL/Verilog Programming, Computer Architecture, FPGA-based System Design, VLSI Design, Embedded Systems, Signal Processing, and Advanced Electronics.

CERTIFICATES