

# Noni Laatz

Physical Design Engineer

✉ [noni.laatz@gmail.com](mailto:noni.laatz@gmail.com)  
☎ (541) 357-4909  
📍 123 Maple Street, Portland,  
ME 04101

## Education

**Bachelor of Science in  
Electrical Engineering at  
University of Maine, Orono,  
ME**

Aug 2018 - May 2022  
Relevant Coursework: Circuit  
Analysis, Signals and  
Systems, Electromagnetics,  
Power Electronics, Control  
Systems, Digital Logic Design,  
Microprocessors, Embedded  
Systems, and Communication  
Systems.

## Links

[linkedin.com/in/nonilaatz](https://www.linkedin.com/in/nonilaatz)

## Skills

Cadence Virtuoso  
Synopsys ICC  
Calibre DRC/LVS  
HSPICE Simulation  
Tcl Scripting  
Static Timing Analysis  
Floorplanning

## Languages

English  
Indonesian

## Profile

Dedicated Physical Design Engineer with 1 year of experience in designing and optimizing integrated circuits. Proficient in EDA tools, floor planning, and physical verification, with a strong understanding of CMOS process technology. Adept at collaborating with cross-functional teams to achieve project goals while contributing to continuous improvement efforts. Demonstrated ability to deliver high-quality results on time and within budget.

## Employment History

### Physical Design Engineer at ON Semiconductor, ME

- May 2023 - Present
- Reduced overall chip area by 15% through optimization of floorplanning and placement strategies, resulting in significant cost savings for ON Semiconductor.
  - Implemented a new power grid design methodology that decreased IR drop by 20%, leading to improved performance and reliability of ON Semiconductor's products.
  - Successfully led a team of 5 engineers in the completion of 3 complex physical design projects within tight deadlines, contributing to a 10% increase in annual revenue for the company.
  - Developed and executed an innovative clock tree synthesis approach that reduced clock skew by 25%, enhancing the performance and efficiency of ON Semiconductor's chips.

### Associate Physical Design Engineer at Texas Instruments, ME

- Jul 2022 - Apr 2023
- Successfully designed and implemented a power-efficient System-on-Chip (SoC) layout for a high-performance microcontroller, resulting in a 15% reduction in power consumption and a 10% increase in overall performance.
  - Led a team of 5 engineers in the development and verification of a high-speed mixed-signal integrated circuit (IC) design, which achieved first-pass silicon success and reduced time-to-market by 20%.
  - Optimized the physical design flow for a complex digital signal processor (DSP) project, reducing the design cycle time by 25% and achieving a 12% improvement in area utilization.

## Certificates

### Certified Physical Design Engineer (CPDE)

Dec 2021

### IPC Certified Interconnect Designer (CID)

May 2020

## Memberships